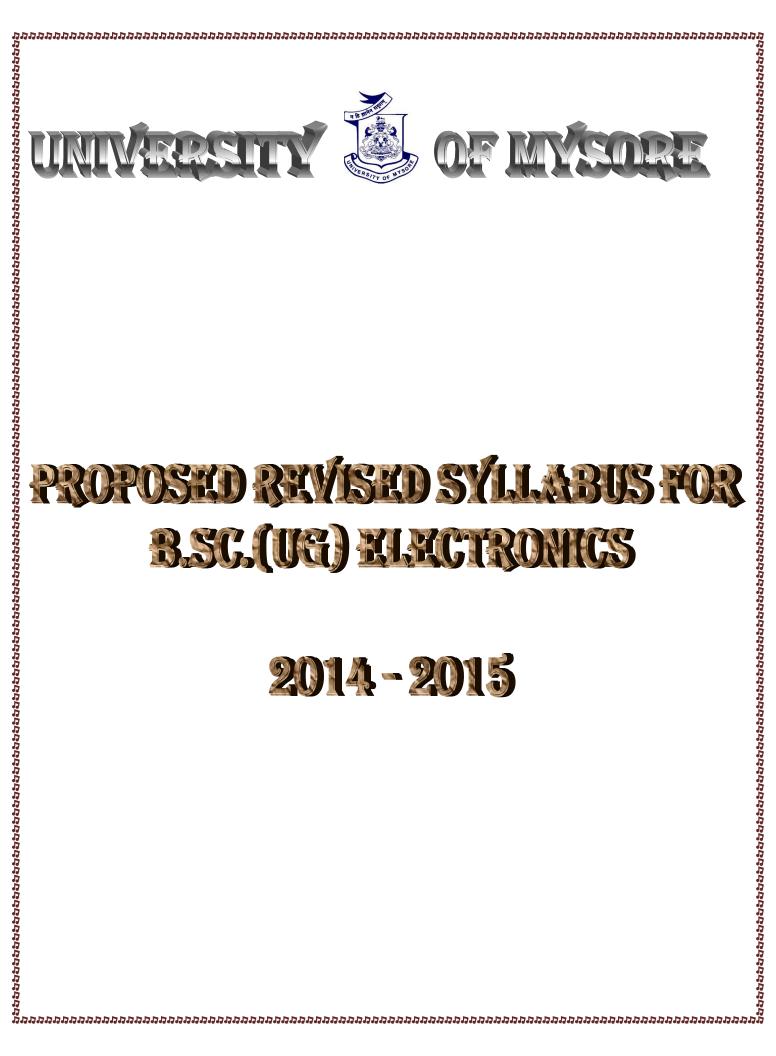


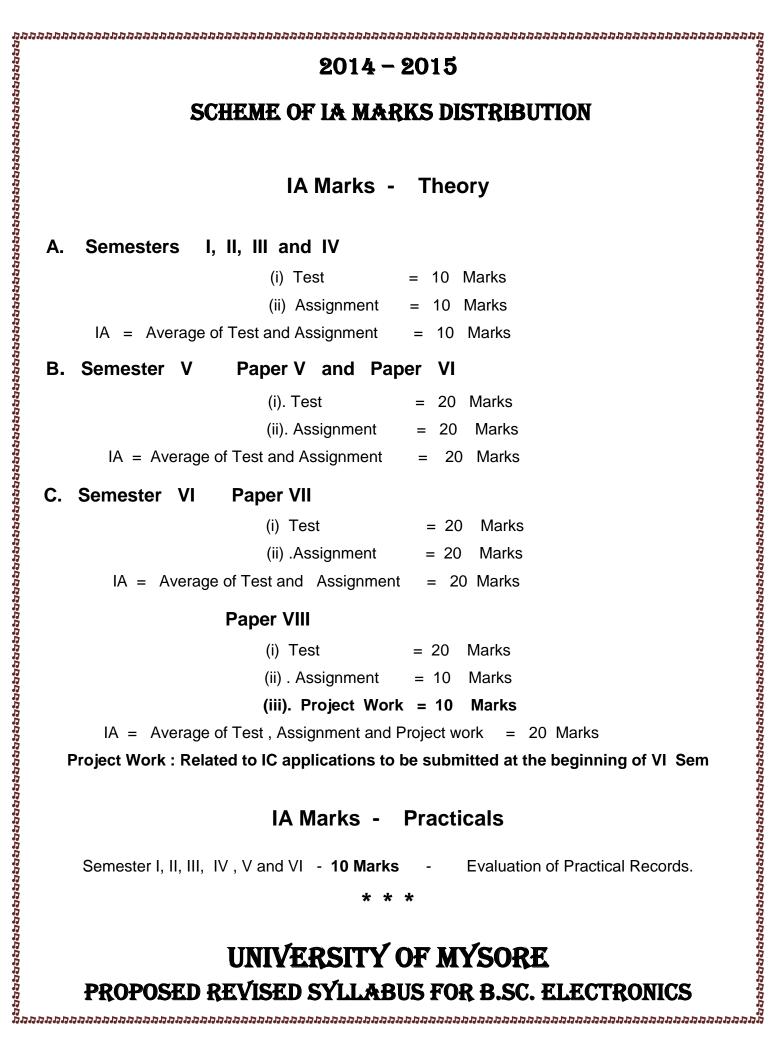
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		2014 - 20	015			
2014 – 2015 SUBJECTS & PAPER CODE Semester Code Title of the Subject – Theory Code Title of the Subject - Practical I EL 1.0 Basic Electronics and Network Theorems ELP 1.0 Basic Electronics and Network Theorems						
Semester	Code	Title of the Subject – Theory	Code	Title of the Subject - Practical		
I	EL 1.0	Basic Electronics and Network Theorems	ELP 1.0	Basic Electronics and Network Theorems Lab		
II	EL 2.0	Amplifiers and Oscillators	ELP 2.0	Amplifiers and Oscillators Lab		
Ш	EL 3.0	Integrated Circuits and Operational Amplifiers	ELP 3.0	Integrated Circuits and Operational Amplifiers Lab		
IV	EL 4.0	Transducers, Instrumentation and Programming in C	ELP 4.0	Transducers, Instrumentation and C Programming Lab		
v	EL 5.1	Digital Electronics and Microcontroller	ELP 5.1	Digital Electronics and Microcontroller Lab		
	EL 5.2	VHDL	ELP 5.2	VHDL Lab		
VI	EL 6.1	Communication	ELP 6.1	Communication Lab		
	EL 6.2.1	Signals and Systems	ELP 6.2.1	Signals and Systems Lab		
٠	EL 6.2.2	Electronic Circuit Design	ELP 6.2.2	Electronic Circuit Design Lab		
•	EL 6.2.3	Programming in C + +	ELP 6.2.3	C + + Programming Lab		
EI 6.2.3	not to be	2.3 are Electives opted by students of Computer * * * UNIVERSITY OF ED REVISED SYLLABUS	T MYS	ORE		

	2014 - 2015 SCHEME OF EXAMINATION										
			SCHEME O	т£	XAN	AIN AT	ION				
Sem	em Paper Code		ode Title of in Hours								
	-		Code Title of the Paper				I <i>A</i> Mai		Exa Ma		Total
				Th	Pr	Exam	Th	Pr	Th	Pr	
I	I	EL 1.0	Basic Electronics and Network Theorems	3	3	3	10	10	60	20	100
II	II	EL 2.0	Amplifiers and Oscillators	3	3	3	10	10	60	20	100
III	111	EL 3.0	Integrated Circuits and Operational Amplifiers	3	3	3	10	10	60	20	100
IV	IV	EL 4.0	Transducers, Instrumentation and Programming in C	3	3	3	10	10	60	20	100
V	v	EL 5.1	Digital Electronics and Microcontroller	3	2	3	20	10	80	40	100 +50
	VI	EL 5.2	VHDL	3	2	3	20	10	80	40	100 +50
	VII	EL 6.1	Communication	3	2	3	20	10	80	40	100 +50
		EL	Signals and								100
VI		6.2.1	Systems Electronic	3	2	3	20	10	80	40	+50
	•	6.2.2	Circuit Design	3	2	3	20	10	80	40	+50
	•	EL 6.2.3	Programming in C + +	3	2	3	20	10	80	40	100 +50
•	El 6.2.2 a El 6.2.3	and El 6.2 not to be	Electronics and Microcontroller VHDL Communication Signals and Systems Electronic Circuit Design Programming in C + + .3 are Electives opted by students of UNIVERSI REVISED SYL	Comp *	outer S *	Science as	s one of	the op	tional		
	PRO	POSED	UNIVERSI REVISED SYL	TÝ L a b	OF US	MÝS FOR B	ORE .sc. I	ELEC	TRO	NICS	



	2014 - 2015	
QUESTION P	PAPER PATTERN – MA	ARKS DISTRIBUTION
SEMESTERS	I, II, III & IV	
► There will	be three Parts A, B and C.	
 Part A is fr 	rom Unit 1, Part B is from Unit 2 a	and Part C is from Unit 3.
Each Part	- 20 marks	
	PART A , B and C	
Each Part Mar		
1. 2 mark questio	ons – Total 3 To be answered	2 2 × 2 = 4 marks
2. 6 mark questio	ons – Total 3 To be answered	2 6 × 2 = 12 marks
3. 4 mark proble	ems – Total 3 To be answered	1 4 × 1 = 4 marks
	Each Part	Total = 20 marks
Grand T	otal (A + B + C)	60 marks
SEMESTERS	V & VI	
► There will b	be four Parts A, B , C and D	
 Part A is fr 	rom Unit 1, Part B is from Unit 2 ,	Part C is from Unit 3 and
Part D is fi	rom all Unit 1, Unit 2 & Unit 3.	
Each Part	- 20 marks	
	PART A , B , C and D	
Each Part Mark	ks Distribution	
1. 2 mark questions	– Total 3 To be answered 2	$2 \times 2 = 4$ marks
2.6 mark questions	a – Total 3 To be answered 2	6 × 2 = 12 marks
3. 4 mark problems	s – Total 3 To be answered 1	$4 \times 1 = 4$ marks
_	Each Part	Total = 20 marks
Grand Tota	aI(A+B+C+D)	80 marks
	* * *	
T	UNIVERSITY OF MY	ÝSORE
	· · ·	R B.SC. ELECTRONICS

Grand Total (A + B	+ (C + D)	80 ma	arks	
		Each Part		Total =	20 marks
3. 4 mark problems – Total	3	To be answered	1	4 × 1 =	4 marks
2. 6 mark questions – Total	3	To be answered	2	6 × 2 =	12 marks
1. 2 mark questions – Total	3	To be answered	2	2 × 2 =	4 marks

						201	4 - 2	2015	5					
	C	QUES	TION	PA	PER	PAT	FERN	1 – M	ARK	s di	STRI	BUTI	ON	
			Part A Unit 1			Part B Unit 2			Part C Unit 3		Un	Part D hit (1+2-	+3)	
Sem Paper	Paper	DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD		Question Numbers		Question Numbers			Question Numbers			Total Marks		
		1 a,b,c	2 a,b,c	3 a,b,c	4 a,b,c	5 a,b,c	6 a,b,c	7 a,b,c	8 a,b,c	9 a,b,c	10 a,b,c	11 a,b,c	12 a,b,c	
		2 Marks	6 Marks	4 Marks	2 Marks	6 Marks	4 Marks	2 Marks	6 Marks	4 Marks	2 Marks	6 Marks	4 Marks	
I	I	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	-	-	-	60
II	II	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	-	-	-	60
Ξ	III	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	-	-	-	60
IV	IV	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	-	-	-	60
v	V	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	80
	VI	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	80
VI	VII	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	80
	VIII	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	2/3	2/3	1/3	80
Sub Sub Sub	odivision odivision odivision	n a - n b - n c -	2 mark 6 mark 4 mark	s - Sh s - De s - P	nort ans escripti roblem	swer qu ve ans	uestion wer quo * *	estion *						
	IV V VI VII VIII odivision odivision	P	ROPOS	l Sed Ri	U NIV EVISE	ERSI D SYL	TY O Labu	of My Is for	SOR B.SC.	E ELEC	TRON	ICS		

			2014	- 2015		
	SC	HEME OF PRACTICAL	EXAM	UNATION MARKS DISTRIBUTION	ON	
				Marks Distribution		Total
Sem	Paper	Title of the Paper		Subdivision	Marks	Marks
		Basic Electronics and				
I		Network Theorems	1.	Formula	02	
		Amplifiers and	2.	Circuit diagram,		
II	Ш	Oscillators		Tabular column, Nature of	03	
111		Integrated Circuits		graph		20
		and Operational	3.	Circuit connections,	05	
		Amplifiers.	_	Setting, Taking readings		
		Transducers and	4.	Calculation, graph,	05	
IV	IV	Instrumentation		result,	05	
			_	accuracy, unit		
			5.	Viva		
		Mieroprocess	1.	Program Writing	05	
		Microprocessor	2.	Entering and	05	20
		and	2	Execution	05	
		C Programming	3.	Verification, Result Viva	05	
			<u>4.</u> 1.			
	v	Digital Electronics	1.	Circuit , Pin diag, Truth table / Program Writing,	15	
	v	Digital Electronics and		Entering	10	
v	Microcontroller	2.	Circuit	10	40	
	When be offer one	۷.	Connection/Execution	05	40	
			3.	Result / Verification,	05	
			5.	result		
			4.	Viva		
			1.	Program Writing,		
	VI	VHDL	••	Circuit diag. Truth tab,	15	40
	••			Waveform, Entering	10	
			2.	Execution	10	
			3.	Result, graph	05	
			4.	Viva		
			1.	Formula, Circuit,		
				Tabular column, Nature of	15	
	VII	Communication		graph		
			2.	Circuit connections,	10	40
				Setting, Taking readings,	10	
VI				graph	05	
			3.	Calculation,		
				graph,result, unit		
			4.	Viva		
			1.	Program Writing,	15	
	•	Signals		Entering	10	40
	VIII	And	2.	Execution	10	
		Systems	3.	Verification, result,	05	
			_	graph		
			4.	Viva		
			1.	Formula, Circuit		
				diagram, tabular column,		40

▲		nature of graph, Designing	15	
▼ (Elective	Circuit Design	2. Connections,	10	
	·/	Simulation	10	
		3. Calculation, Result,	05	
		graph,unit		
		4. Viva		
		1. Program Writing,	15	
	C++	Entering 2 Execution	10	4
▼ (Electiva	Programming	3 Result	05	
(Elective	÷)	4. Viva	00	
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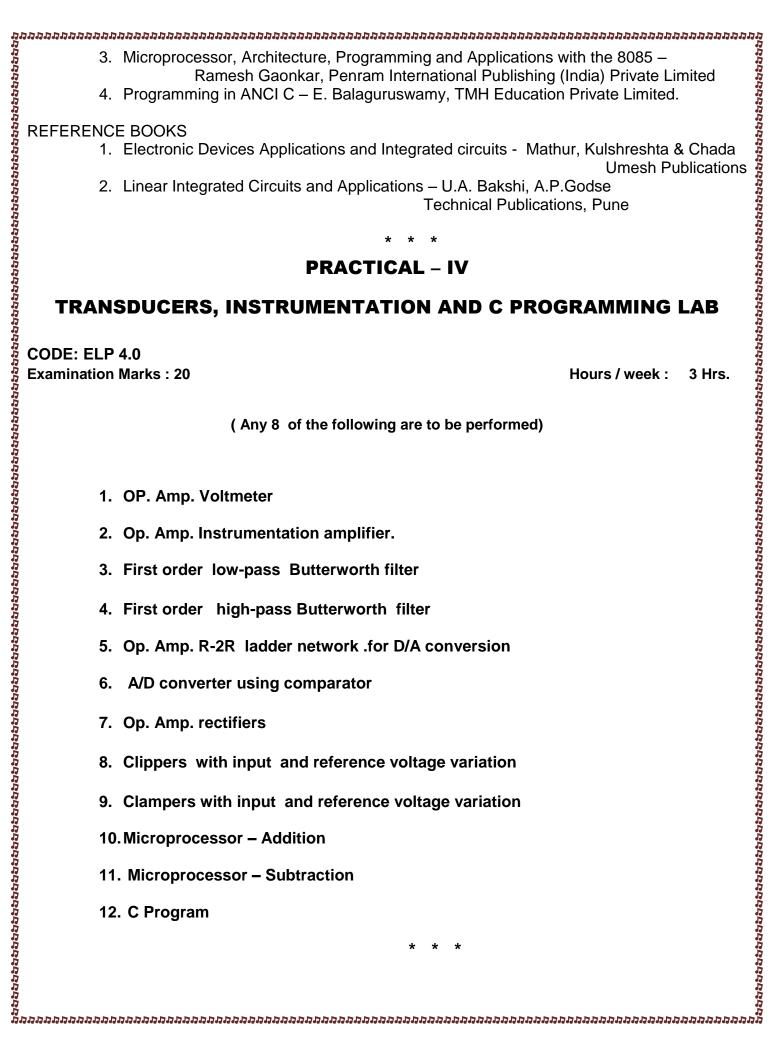
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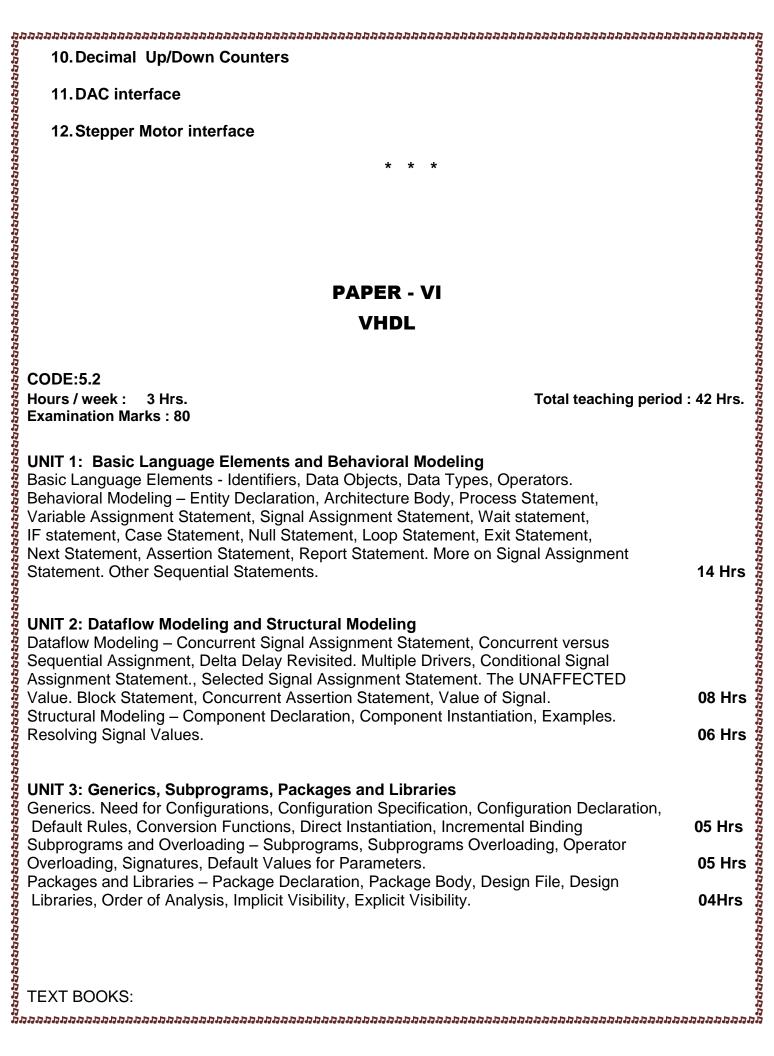
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PAP	PER - V	
DIGITAL ELECTRONICS	AND MICROCONTROLLER	
CODE: EL 5.1		
Hours / week : 3 Hrs.	Total teaching p	period : 42 Hrs
Examination Marks : 80		
UNIT 1: Digital Electronics		
Binary Codes – Weighted and Non-weighted cod		
EXCESS – 3 codesConversion between Binary Parity generators and checkers.	y and Gray codes. Parity codes.	04Hrs
Binary Adders and Subtractors. Multiplexers, Dec	coder and Encoder	04013
Simplification of Boolean expressions – using Bo		05Hrs
Logic families – TTL and CMOS - NAND and NC	OR gates.	
Flip-flops, Shift registers, Counters. Memory – ty	pes, RAM and ROM. Problems	05Hrs
UNIT 2: Microcontroller – 8051 - Architecture.		
Number System – Binary, Octal and Hexadecima		
Conversions Binary Subtraction by 1's and 2's co	•	06Hrs
Microcontroller 8051 – Pin configuration, Ports, R	Registers,	08Hrs
Timers and counters, Interrupts, Memory,		UORIS
UNIT 3: Programming – Microcontroller – 805	51	
8051 Addressing modes and moving data	_	
Arithmetic , Logical, and Jump operations,	Programs	08Hrs
Counter , Timer Programming, Interrupt Program Interfacing with external devices. – DAC and Ste		06Hrs
incontaing with external devices DAO and Ole		
TEXT BOOKS:		
1. Digital Principles and Applications – Albert	t Paul Malvino and Donald P Leach M	cGrawHill
2. Modern Digital Electronics – R. P. Jain – T	TMH Publishing Company Limited	
2 The OOF1 Mierre constraller and Ershedded (Systems – Mohammed Ali Mazidi and	

8051 Addressing modes and moving data	
Arithmetic, Logical, and Jump operations,	Programs
Counter, Timer Programming, Interrupt Prog	ramming.
Interfacing with external devices DAC and	Stepper Motor.

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 PAPER - FUIL

 (Jectroire)

 Determining of the second of th

1. Op-Amps and Linear Inte	egrated Circuits	•
2 Papia Flastronica Calid S	toto DI Thoroi	Pearson Education Asia
	•	a - S Chand And Company Ltd /cgraw-Hill Publishing Company Limited, New Delh
(Note: Variations	s of the above b	ooks may be adopted appropriately)
		* * *
	PRACT	ICAL – VIII
	(Ele	ective)
E	lectronic Ci	rcuit Design Lab
	(Using	J PSPICE)
ODE:ELP 6.2.2		
kamination Marks : 40		Hours / week : 3 hrs.
(Any 8 o	f the following are	e to be performed using Pspice)
1. Design and Simulati	on of diode Hall	f-Wave Rectifier / Full-Wave Rectifier
2. Design and Simulati	on of diode Bric	Ige Rectifier
3. Design and simulati	on of CE amplifi	er
4. Design and Simulati	on of Op. Amp.	- Inverting amplifier (ac/dc)
5. Design and Simulati	on of Op. Amp.	- Non-Inverting amplifier (ac/dc)
6. Design and Simulati	on of Op. Amp.	adder for a given output
7. Design and Simulati	on of Op. Amp.	Butterworth First order low-pass filter
8. Design and Simulati	on of Op. Amp.	Butterworth First order high-pass filter
9. Design and Simulati	on of 555 Time	r – Astable multivibrator
10. Design and Simulati	on of 555 Time	r – Monostable multivibrator
11. Design and Simulati	on of 555 Time	r – Frequency divider circuit.
12. Design and Simulat	ion of Op. Amp	. Analog Computational Circuit

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EL1.1 MODEL OUESTION PAPER L Semester B.S.c. Examination, Nov / Dec 2013 (genester B.S.c. Examination, Nov / Dec 2013 (genester Scheme, 2014 - 2015 onwards) Electronics Basic Electronics and Network Theorems Time: 3 Hours Max. Marks: 60 </t

